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| 09/772,920 | 01/31/2001 | Lawrence A. Clevenger | Y0999492 | 9976 |

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MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

| EXAMINER | |
|---|---|
| KESHAVAN, BELUR V | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/772,920 | Applicant(s) CLEVENGER ET AL. | |
|---|---|---|---|
| | Examiner Belur V Keshavan | Art Unit 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Status Of Claims*

Claims 1-16 and 18-34 are in the application.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims1- 4 are rejected under 35 U.S.C. 102(b) as being anticipated by McTeer (U.S. Patent No.5,939,788).

Regarding claims 1, 3 and 4, McTeer discloses, in column 23 and in figure 16, a method of forming an interconnect on a semiconductor substrate (10), comprising: forming relatively narrow first structure at the bottom of the dual damascene structure in a dielectric (14) formed on the semiconductor substrate; forming a relatively wider second structure at the top of the dual damascene structure in the dielectric formed on the semiconductor substrate; forming a liner (2) comprising aluminum and titanium nitride (line 48) in the first and the second structures such that the first structure is substantially filled and the second structure is substantially unfilled; and forming a metallization (3) comprising copper (line 50) over the liner to fill completely the second structure.

Regarding claim 2, McTeer discloses, in column 17 and lines 46-47, wherein the liner is deposited by PVD.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 21and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over McTeer in view of Parikh (U.S. Patent No. 6,225,207).

Regarding claim 21 and 22, McTerr anticipates claim 1 as above but lacks forming the relatively narrow first structure not being connected to the relatively wider second structure and forming the wider second structure on the substrate apart from the relatively narrow first structure. However, Parikh teaches, in column 11, lines 31 and figure 5D (554 and 552), forming the relatively narrow first structure (554) not being connected to the relatively wider second structure (552) and forming the wider second structure on the substrate apart from the relatively narrow first structure. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of McTeer with that of Parikh to form

an interconnect on a semiconductor substrate with different design requirements, wider structure to carry large currents and narrow structure for transmitting signals.

Claims 5-15, 23, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Parikh.

Regarding claims 5, 6, 8, 9,10, 11-14, Parikh discloses, in columns 14, 15and 16 and in figures 9A-9F, a method of forming an interconnect on a semiconductor substrate comprising: forming a contact (940) including a slot (924) in a dielectric (916) comprising an oxide and low K polymer dielectric (column 15, lines 37-42) formed on a semiconductor substrate (910); forming troughs (938) into the dielectric structure; depositing a conducting material comprising CVD or PVD tungsten on the dielectric, depositing a metal comprising copper over the conducting material in column 16 and lines 51-57; adjusting the thickness of the metal to fill completely the slot and troughs, in column 15 and lines 11-13; removing the conducting material and the metal back to the dielectric (916) and selectively removing the conducting material by CMP or etching, in column 15, and lines 14-17 and in column 16 and lines 20-21.

Regarding claim 7, Parikh discloses, in column 15 and lines 19 –20, contacts (952) comprise contacts formed between first and second metal levels formed on the semiconductor substrate.

Regarding claim 15, Parikh teaches in the abstract that multiple damascene structure which comprises repeating the deposition of the conducting material and the metal on the resulting structure.

Regarding claims 23 and 24, Parikh teaches, in column 11, lines 31 and figure 9F forming the contact (952) not being connected to the trough (956) and forming the trough in the dielectric on the substrate apart from the contact.

Claims 16, 18, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Parikh

Regarding Claims 16, 18, 19 and 20, Parikh discloses, in columns 14, 15and 16 and in figures 9A-9F, a method of forming an interconnect on a semiconductor substrate comprising: forming troughs (956) between the first and second metal levels, including a slot (950) in a dielectric formed on a semiconductor substrate; forming contacts (952) in the dielectric comprising contacts formed between the first and the second metal levels formed on the semiconductor substrate, thereby to form a dual damascene structure; depositing a conducting material in the dielectric by CVD ; depositing a metal over the conducting material to fill the slot and the troughs; removing the metal either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric and selectively removing the conducting material by selective etch

## Remarks

### *Amendment*

The examiner has noted amendment to claim 10 wherein the word "completely" has been replaced by the word "substantially". The examiner has withdrawn the objection to claim 10.

### *Applicants' arguments*

Applicants' arguments filed 07/09/2003 have been fully considered but they are not persuasive.

Regarding the McTeer and the Parikh references the examiner notes the applicants' argument that there are elements of the claimed invention, which are not found in McTeer and in Parikh.

Although McTeer is silent with respect top and bottom, the damascene structure shown in figure 16 shows a relatively narrow first structure opening near the bottom in the dielectric layer (14) formed on a semiconductor substrate (10) with a relatively wider second structure opening near the top of the dielectric layer. McTeer teaches formation of a damascene structure as shown in figure 16 with a narrower via with a wider trench contacting the via in the same dielectric (14) formed on the semiconductor substrate (10). Further McTeer discloses forming a liner (2) comprising aluminum and titanium nitride (line 48 in column 23) deposited by the well known PVD or CVD techniques (line 57-50 in column 22) in the narrow and in the wider structures such that the narrow structure is substantially filled and the wider structure is substantially unfilled.

In view of the above, applicants' argument that there are elements of the claimed invention, which are not found in McTeer is not persuasive.

Parikh discloses in column 14-16 and in figures 9A-9F depositing a metal comprising copper over the conducting material comprising CVD or PVD tungsten on the dielectric. Copper is a metal and a conducting material. Tungsten is a metal and is a conducting material and WN is a conducting material comprising tungsten. Therefore, Parikh discloses in column 16 and lines 51-57 depositing a conducting material comprising CVD or PVD tungsten on the dielectric and depositing a metal comprising copper over the conducting material to fill completely the slot and troughs. Also Parikh discloses that a suitable liner material for copper comprising damascene structure is a material comprising tungsten. Therefore, Parikh teaches filling completely the slot and troughs with a metal after lining the same with a conductive material.

In the Office Action of 09/04/2002, the examiner objected to claim 10. because of the following informalities: The claim 10, reads "the method of claim 5, wherein a thickness of the conducting material is adjusted so as to completely fill the slot". The examiner understands based on independent claim 5 and figures 2 and 3 that the slot is filled completely with the metal over the conducting material and not completely filled by conducting material as claimed in the dependent claim 10. In response to the objection the applicants have amended claim 10 by replacing the word "completely" with "substantially" commensurate with the independent claim 5 and as per the drawings.

The examiner notes the applicants' argument that the teachings of McTeer and that of Parikh should not be combined in the rejection of claims 21 and 22. Both McTeer and Parikh teach forming interconnect on a semiconductor substrate as given above. The examiner is not persuaded by arguments of the applicants that the teachings should not be combined.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V Keshavan whose telephone number is 703 306 5985. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 703 308 1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308 0956.

Bvk.
August 25, 2003.

Belur V. Keshavan
Examiner. Art Unit 2825.

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800